

## **CLAIM LISTING**

1. (Original) An interconnect apparatus comprising:  
a silicon substrate;  
contact pads processed on the silicon substrate to connect to an integrated circuit (IC) die;  
interconnections selectively interconnecting the contact pads, the interconnections  
processed on the silicon substrate; and  
circuit elements processed on the silicon substrate with the same processing as the  
contact pads and the interconnections to interoperate with the IC die.
2. (Original) An interconnect apparatus according to claim 1, wherein the circuit elements  
comprise a micro electro-mechanical system (MEMS) device.
3. (Original) An interconnect apparatus according to claim 2, wherein the MEMS device  
further includes a microfluidic system.
4. (Original) An interconnect apparatus according to claim 2, wherein the MEMS device  
further includes an actuation circuit device.
5. (Original) An interconnect apparatus according to claim 1, wherein the circuit elements  
comprise a sensor circuit.
6. (Original) An interconnect apparatus according to claim 1, wherein the silicon substrate  
comprises a high-resistivity silicon substrate.
7. (Original) An interconnect apparatus according to claim 6, wherein the circuit elements  
comprise optical circuit components.
8. (Original) An interconnect apparatus according to claim 1, wherein the circuit elements  
comprise an active circuit element.

**9.** (Original) An interconnect apparatus according to claim 1, further comprising a cap processed onto the silicon substrate to hermetically isolate circuit elements on the silicon substrate.

**10.** (Original) An interconnect apparatus according to claim 9, wherein the cap comprises a cap of silicon-based material.

**11.** (Original) An interconnect apparatus according to claim 9, further comprising interconnect vias manufactured in the cap to provide electrical connectivity to contact pads on the silicon substrate.

**12-18. (Canceled)**

**19.** (Original) An integrated circuit chip having a circuit element on a substrate created with a first lithographic processing interconnected on a high-resistivity silicon interconnect substrate having functional circuit elements embedded in the interconnect substrate, created by the process of:

processing contact pads and electrical traces on the silicon substrate with a second lithographic processing to interconnect the circuit elements;

processing the circuit elements on the interconnection substrate with the second lithographic processing; and

interconnecting the circuit element of the first lithographic processing on the separate substrate to contact pads on the interconnection substrate.

**20.** (Original) An integrated circuit chip according to claim 19, wherein the silicon interconnect substrate further includes a micro electro-mechanical system (MEMS) device.

**21.** (Original) An integrated circuit chip according to claim 19, wherein the circuit elements comprise an active circuit element.

**22.** (Original) An integrated circuit chip according to claim 19, wherein the circuit elements on separate substrates comprise circuit elements all on silicon substrates.

**23.** (Original) An integrated circuit chip according to claim 19, wherein the silicon interconnect substrate further comprises a silicon lid to hermetically seal functional circuit elements.

**24.** (Original) An integrated circuit chip according to claim 23, wherein the lid further comprises interconnections through the lid to interconnection contact pads on the silicon interconnect substrate.

**25-28. (Canceled)**

**29.** (Original) An electronic system comprising:  
a chip with an integrated circuit (IC) bonded to contact pads on a silicon interconnect backplane, the silicon backplane having integrated circuits including a micro electro-mechanical system (MEMS) device processed into the silicon backplane with the same processing used to create the contact pads, the processing different from a processing used to create the IC; and  
a direct current power storage cell coupled with the chip to supply power to the chip.

**30.** (Original) A system according to claim 29, wherein the MEMS device further includes a microfluidic system.

**31.** (Original) A system according to claim 29, wherein the MEMS device further includes an actuation circuit device.

**32.** (Original) A system according to claim 29, wherein the circuit elements comprise sensor circuits.

**33.** (Original) A system according to claim 29, further comprising a cap processed onto the silicon backplane to hermetically isolate circuit elements on the silicon backplane.

**34.** (Original) A system according to claim 33, wherein the cap comprises a cap of silicon-based material.

**35.** (Original) A system according to claim 33, further comprising interconnections manufactured through the cap to provide electrical connectivity to contact pads on the silicon backplane.